

KARUNY UNIVERSITY, COIMBATORE, INDIA

DEPARTMENT OF ECE

INTERNATIONAL CONFERENCE ON DEVICES, CIRCUITS AND SYSTEMS (ICDCS – 2012) PROGRAM SCHEDULE

1st DAY : MARCH 15 (THURSDAY), 2012					
REGISTRATION(8:30 AM- 9:30 AM) - ECE BLOCK					
DAY/TIME	CONFERENCE HALL 1 (EA)	CONFERENCE HALL 2 (ECE SH.GF)	CONFERENCE HALL 3 (ECE SH.FF)	CONFERENCE HALL 4 (EMT CH)	CONFERENCE HALL 4 (PL.SF)
9:30 AM- 10:30 AM	INAUGURATION (ELOHIM AUDITORIUM)				
COFFEE BREAK(10:30 AM – 10:45 AM) ELOHIM AUDITORIUM					
10:45 AM – 12:00 PM	<u>KEYNOTE1 (K1)</u> Dr.Jakub Kedzierski , MIT Lincoln Laboratory & Visiting faculty at the Indian Institute of Technology, Bombay. Venue: ELOHIM AUDITORIUM	<u>KEYNOTE 2 (K2)</u> Dr.N.MohanKumar , IEEE- EDS Madras Chair & Professor, S.K.P. Engineering College, Thiruvannamalai. Venue: ECE SH.GF	<u>KEYNOTE 3 (K3)</u> Dr.N.B.Balamurugan , Thiagarajar Engineering College, Madurai. Venue: ECE SH.FF		
LUNCH (12:00 PM-1:30 PM) - JORDAN RESTAURANT					
<u>SESSION 1</u>					
1:30 PM - 3:00 PM	COMMUNICATION(C1) C -Dr.B.Balamurugan CC -Mrs. G.Shinelet	VLSI (V1) C -Dr.N.Mohan Kumar CC – Mr. P. Dinesh Kumar	IMAGE PROCESSING (I1) C – Dr. Amitabh Wahi CC – Mrs. Diana Andrushia	VLSI (V2) C – Dr.P.Vijayakumar CC-Mrs. B. Manjurathi	MEMS/NANO (M1) C – Mr. Mayank CC – Mrs. M.A.P. Manimekalai
COFFEE BREAK (3:00 PM – 3:15 PM) ECE BLOCK GROUND FLOOR					
<u>SESSION 2</u>					
3:15 PM - 4:45 PM	VLSI (V3) C – Dr.N.Mohan Kumar CC – Ms. Evelyn Ezhilarasi	IMAGE PROCESSING (I2) C – Dr. Amitabh Wahi CC – Mrs. Thusnavis Bella Mary	COMMUNICATION (C2) C – Dr.B.Balamurugan CC- Mrs. Mary Neebha	MEMS/NANO (M2) C – Dr. Ravi Shankar CC – Mr. R.S. Suriavel Rao	VLSI (V4) C- Dr. Sivamangai CC – Mr. Manikandan

Note: C-Chair Person; CC-Co Chair

Venue Details:

1. EA- Elohim Auditorium
2. ECE SH.GF- ECE Seminar hall, Ground floor
3. ECE SH.FF- ECE Seminar hall, first floor
4. PL.SF- Placement office, Old Biotech building, Second floor
5. EMT CH- EMT Conference Hall (ECE Block Ground Floor)

KARUNY UNIVERSITY, COIMBATORE, INDIA**DEPARTMENT OF ECE****INTERNATIONAL CONFERENCE ON DEVICES, CIRCUITS AND SYSTEMS (ICDCS – 2012)****PROGRAM SCHEDULE**

2nd DAY : MARCH 16 (FRIDAY),2012					
REGISTRATION(8:30 AM- 9:30 AM) - ECE BLOCK					
DAY/TIME	CONFERENCE HALL 1 (EA)	CONFERENCE HALL 2 (ECE.SH.GF)	CONFERENCE HALL 3 (ECE.SH.FF)	CONFERENCE HALL 4 (EMT CH)	CONFERENCE HALL 4 (PL.SF)
9:30 AM- 10:30 AM	<u>PLENARY TALK</u> DR. V.RAMGOPAL RAO, INSTITUTE CHAIR PROFESSOR, EE DEPARTMENT, IIT BOMBAY Venue : Elohim Auditorium				
COFFEE BREAK(10:30 AM- 10:45AM) ECE BLOCK, GROUND FLOOR					
<u>SESSION 3</u>					
10:45AM - 12:15PM	EMBEDDED SYSTEM (E1) C – Dr. C. Palanisamy CC – Mr. Manoj Gopalakrishna Pillai	VLSI (V5) C – Dr.D. Jackuline Moni CC – Mrs.Shylu	VLSI (V6) C- Dr. KarthigaiKumar CC – Ms.J.Grace Jency Gnanammal	COMMUNICATION (C3) C – Dr. Jancsi CC – Mr. S.R. Jino Ramson	VLSI (V7) C – Dr. Sudesh Kumar CC – Mr.Shajin Prince
LUNCH(12:15 PM- 1:30 PM) -- JORDAN RESTAURANT					
<u>SESSION 4</u>					
1:30 PM- 3:00 PM	IMAGE PROCESSING (I3) C – Dr. J. Dinesh Peter CC– Mr.Jagannath.D.J	COMMUNICATION (C4) C – Dr.G. Josemin Bala CC– S. Greeta Priyadharshini	SIGNAL PROCESSING (S1) C – Dr. J. Ramesh CC– Mr.S. Dhanasekar	IMAGE PROCESSING (I4) C – Dr. C. Palanisamy CC – Mr. Sathesh .A	VLSI (V8) C – Dr. A. Rajeswari CC – Mr.A Amir Anton Jone
COFFEE BREAK(3:00 PM-3:15 PM) ECE BLOCK GROUND FLOOR					
3:15 PM 3.45 PM	CLOSING CEREMONY (ECE SEMINAR HALL GROUND FLOOR)				

Note: C-Chair Person; CC-Co Chair**Venue Details:**

1. EA- Elohim Auditorium
2. ECE SH.GF- ECE Seminar hall, Ground floor
3. ECE SH.FF- ECE Seminar hall, first floor
4. PL.SF- Placement office, Old Biotech building, Second floor
5. EMT CH- EMT Conference Hall (ECE Block Ground Floor)

SESSION 1COMMUNICATION(C1)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	12	Optical Phase Conjugation in Long haul Optical Transmission Authors: Sridarshini Thirumaran and Pradeep Doss M	1. SRIDARSHINI THIRUMARAN, 2. S.K NITHILA DEVI, 3. P.DEEPIKA 4. A VASANTHI
2	41	A Proposed Lateral Ddr Impatt Structure For Better Millimeter-Wave Optical Interaction Authors: Aritra Acharyya and J. P. Banerjee	1. ARITRA ACHARYYA
3	44	Maximization Battery Lifetime and Improving Efficiency Authors: J.S. Sathiyarayanan and Dr A.Senthil Kumar	1. J.S. SATHIYANARAYANAN
4	65	Electromagnetic and Laplace domain analysis of Memristance and Associative learning using Memristive Synapses modeled in SPICE Authors: Rajkumar Chinnakonda Kubendran	1. RAJKUMAR KUBENDRAN
5	66	Novel Technique for PAPR Reduction in OFDM System using $\pi/4$ -Shifted-DQPSK Modulation & Turbo Code Authors: Kavita Bani and Rajesh Bansode	1. RAJESH S. BANSODE, 2. KAVITA BANI
6	67	Ergodic Channel Capacity of WiMAX OFDM Networks in the Presence of Adjacent Channel Interference with Diversity Combining Authors: S.Thai Subha and Vidhyacharan Bhaskar	1. S.THAI SUBHA
7	82	S-Band Receiver Front-End Design for Portable Satellite Ground Terminal Authors: Sudesh Kumar Jain, Jagruti Raval and Dinesh Kumar Singh	1. SUDESH KUMAR JAIN
8	283	SIMO Channel Capacity using Hybrid Diversity Combining Techniques in a Rayleigh Fading Channel Authors: Sai Sindhoori V.R and Vidhyacharan Bhaskar	1. SAI SINDHOORI V. R

VLSI(V1)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	33	"VLSI Signal Processing Oriented Segmentation based Serial Parallel multiplier" Authors: Vandana Ar and Uma A	1. VANDANA. AR
2	48	Accurate Power Measurement Methodology for VLSI Circuits Using CAD Tools Authors: Dr Veena Chakravarthi, Ajay G and Ramya Sunderrajan	1. AJAY G, 2. RAMYA SUNDERRAJAN
3	55	Analytical expression for storage time and injection ratio of a non-uniformly doped n-Si SBD Authors: Md. Imran Momtaz and M. M. Shahidul Hassan	1. MD. IMRAN MOMTAZ
4	61	Complex Orthogonal Space-Time Block Codes Rates 3/7 ,4/8 and 6/8for 3 ,4 and4Transmit Antennas in Space Time Coding Authors: Satyanara Murthy	1. N. SATYANARAYANA MURTHY
5	74	Dual Carrier Modulation Technique Using Matlab For A Five Level Inverter Authors: K.Kaviarasu, K.Karthikeyan, S.Balamurugan, A.Kaja Moideen, Mr.G.Ayappan	1. K.KAVIARASU, 2. K.KARTHIKEYAN, 3. S.BALAMURUGAN, 4. A.KAJA MOIDEEN, 5. MR.G.AYAPPAN
6	79	A Novel VLSI Architecture for Generation of Six Phase Pulse Compression Sequences Authors: Pechetty Tirumala Rao, Siva Kumar, Chukka Ramesh and Yelaka Madhu Babu	1. P.TIRUMALA RAO
7	344	Efficient Design 2k-1 Binary to Residue Converter Authors: Radha Shende, Pravin Zode and Pradnya Zode	1. PRADNYA ZODE, 2. RADHA SHENDE, 3. PRAVIN ZODE
8	89	Threshold voltage and I-V Characteristics of Cylindrical, Surrounding- Electrolyte ISFET Authors: Jiten Ch. Dutta and Phibadondor.S. Warjri	1. PHIBADONDOR .S.WARJRI

IMAGE PROCESSING(I1)

S.NO	Paper ID	Title	REGISTERED AUTHORS
1	75	A FUSION TECHNIQUE FOR MEDICAL IMAGE SEGMENTATION Authors: Uma Maheswari, Dr. G. Radhamani	1.J. UMAMAHESWARI
2	96	Forgery Detection in Digital Images Using Self Organizing Map Authors: Merylin Smily Ruth. R, Vanitha L and Fredrick Gnanaraj.F	1.MERYLIN SMILY RUTH. R. 2.FREDRICK GNANARAJ. F.
3	99	MULTIPLE NOISE REDUCTION USING HYBRID METHOD FOR LEAF RECOGNITION Authors: Valliammal Ponnarayan, Dr. S. N. Geethalakshmi	1.N.VALLIAMMAL
4	101	IMPLEMENTATION OF SOC'S AUDIO VIDEO COPROCESSOR Authors: Krishna Karthik Tatineni, Praveen Blessington T and Dr Bhanu Murthy Bhaskara	1.KRISHNA KARTHIK. T
5	104	A 1.2V 10 bit 80MS/S sample and hold for ADC applications Authors: Sunil Gavaskar Reddy Yelaka and Liter Siek	1.Y.SUNIL GAVASKAR REDDY
6	174	COMBINED APPROACH OF USER SPECIFIED TAGS AND CONTENT-BASED IMAGE ANNOTATION Authors: Vivitha Vijay and I. Jeena Jacob	I.JEENA JACOB
7	187	An Embedded Architecture for Implementation of a Video Acquisition Module of a Smart Camera System Authors : Jai Gopal Pandey, Abhijit Karmakar and Chandra Shekhar	1.JAI GOPAL PANDEY

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	91	Modeling of Enzyme Biosensor based on pH-sensitive Field Effect Transistor for detection of Glucose Authors: <u>Jiten Ch. Dutta and Monalisa Hazarika</u>	1. MONALISA HAZARIKA
2	373	Input /Output Peripheral Devices Control Through Serial Communication Using MicroBlaze Processor Authors: <u>Muralikrishna Boppana and Gnana Deepika</u>	1.B.MURALIKRISHNA, 2.K.GNANA DEEPIKA
3	106	Four Bit CMOS Full Adder in Submicron Technology with Low Leakage and Ground Bounce Noise Reduction Authors: <u>Jayashree Hv and Harsha K</u>	1.HARSHA K
4	383	Compact packing of CdS variable size nanoparticle in flower like TiO ₂ nanorods for solar cell Authors: <u>Mrinmoy Misra and Madan Lal Singla</u>	1.MRINMOY MISRA
5	113	64-bits Low Power CMOS SRAM by using 9T Cell and Charge Recycling Scheme Authors: <u>Varun Kumar Singhal and Balwinder Singh</u>	1.VARUN KUMAR SINGHAL
6	121	A Power Efficient and Constant-gm 1.8 V CMOS Operational Transconductance Amplifier with Rail-to-Rail Input and Output Ranges for Charge Pump in Phase-Locked Loop Authors: <u>Manas Kumar Hati and Tarun Kanti Bhattacharyya</u>	1.MANAS KUMAR HATI
7	122	Control Methods For Four-Leg Voltage Source Inverter Authors: <u>N. Amutha Priya and M. Carolin Mabel</u>	1.M. CAROLIN MABEL
8	388	Realization of Fractional Order Differentegrals. Authors: <u>Rutuja Dive and Mohan Aware</u>	1.RUTUJA DIVE
9	202	Two Dimensional Analytical Potential Distribution Model for GaN MESFET Authors: <u>Tanvir Ahmed, Md. Tanjib Atique Khan and Md. Shafiqul Islam</u>	1.TANVIR AHMED

MEMS/NANO(M1)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	285	Evidence of Hysteresis from First Principle DFT Simulations of I-V Curves in Pt/TiO ₂ -x – TiO ₂ /Pt Memristive Systems Authors : Mayank Chakraverty and Harish Mallikarjun Kittur	1.MAYANK CHAKRAVERTY
2	98	Sensitivity Analysis On MEMS Capacitive Differential Pressure Sensor For Aerospace Application Authors: Eswaran P	1.ESWARAN.P
3	100	A 10-bit 1-GS/s current-steering DAC with Carbon Nanotube Field Effect transistor (CNFET) Authors: Parisa Moslehi-Nejad, Ali Shakhoseini and Behruz Behtoe	1.P.MOSLEHI-NEJAD
4	107	The Non-Equilibrium Green's Function (NEGF) Simulation of Nanoscale Lightly Doped Drain and Source Double Gate MOSFETs Authors : Zahra Rajabi, Ali Shakhoseini and Rahim Faez	1.Z. RAJABI
5	190	Design and Simulation of AlGa _N /Ga _N HFET Authors : Shevin Varughese and Nirmal D	1.SHEVIN BOBIN VARUGHESE
6	240	Mixed Mode Simulation Of SRAM Finfets Authors : I Flavia Princess Nesamani, M Manikandan, P Sindhu and Dr.V Lakshmiprabha	1.P SINDHU, 2.M.MANIKANDAN
7	392	Simulation Studies of Negative Bias Temperature Instability in FinFETs using Two-Stage model Authors : Narendiran Anandan and Bindu Bobby	1.NARENDIRAN A
8	393	Reliability Studies of AlGa _N /Ga _N High Electron Mobility Transistors (HEMT) Authors : Nandha Kumar S and Bindu Bobby	1.NANDHA KUMAR S
9	366	OPTICALLY CONTROLLED REFLECTION TYPE RF PHASE SHIFTER USING RAT-RACE COUPLER ON SILICON SUBSTRATE Authors: AVANISH BHADAURIA	1. AVANISH BHADAURIA

SESSION2

VLSI(V3)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	129	Handwritten Farsi Numeral Recognition by Neural Network Based on Single Electron Transistors (SETs) Authors: Maryam Najafi, Ali Shahhoseini and Sattar Mirzakuchaki	1.MARYAM NAJAFI
2	130	A new cell with hybrid single electron transistor and MOS transistor with feedback technique Authors: Sajjad Mosavi, Ali Shahhoseini and Hossein Shamsi	1.SAJJAD MOSAVI
3	137	A 0.5 V, 20 μ W Pseudo differential 500 kHz Gm-C Low Pass Filter in 0.18 μ m CMOS Technology. Authors: Vasantha Harishchandra and Tonse Laxminidhi	1.VASANTHA M.HARISHCHANDRA
4	139	Design of CMOS Class E Power Amplifier for WLAN and Bluetooth Applications Authors: Ribu Mathew	1.RIBU MATHEW
5	140	Analysis and study of different parameters affecting the I-V characteristics of Tunnel-FET Transistor Authors: Partha Sarathi Gupta, Sayan Kanungo, Hafizur Rahaman and Partha Sarathi Dasgupta	1. SAYAN KANUNGO
6	145	Implementation of BIST controller for fault detection in CLB of FPGA Authors: Jamuna S and Agrawal Vk	1.JAMUNA S
7	146	Design of a 2.3 GHz Low Noise Amplifier for WIMAX applications Authors: Anup Jyoti Deka, Ishaan Biswas and S C Bose	1.ISHAAN BISWAS, 2. ANUP JYOTI DEKA
8	153	Base Transit Time of a Heterojunction Bipolar Transistor (HBT) with Gaussian Doped Base Under High-Level of Injection Authors: S. M. Moududul Islam, Md. Iqbal Bahar Chowdhury, Yeasir Arafat and Md. Ziaur Rahman Khan	1.S. M. MOUDUDUL ISLAM
9	207	Silicon vs. Germanium Junctionless Double-Gate Field Effect Transistors Authors: Ratul Kumar Baruah	1.RATUL KUMAR BARUAH
10	368	Architectural Design of a Highly Programmable Radix-2 FFT Processor with Efficient Addressing Logic Authors: Saikat Kumar Shome, Abhinav Ashesh, Durgesh Kumar Gupta and Siva Ram Krishna Vadali	1.SAIKAT KUMAR SHOME

IMAGE PROCESSING(12)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	178	Medical Images: Formats, Compression Techniques and DICOM Image Retrieval A Survey Authors: Amol Bhagat and Mohammad Atique	1.A. P. BHAGAT
2	250	Design of an Advanced Signal Conditioning Unit for Sensor with Reduced off-the-Shelf Components Authors: Arun Kumar Sinha[§], Daniele D. Caviglia[§] and Pankaj Gaur*	1.PANKAJ GAUR
3	312	Delay And Power Optimized Register Blocks For The Low Power Microcontrollers Authors: G Rakesh Chowdary, A.L.G.N. Aditya and J. Meenakshi	1.A.L.G.N. ADITYA 2.J. MEENAKSHI
4	317	Control Of Backlash In Electromechanical System-Design And Simulation Based Approach Authors: J Jaisheela and Dr. k Senthil Kumar	1.J JAISHEELA
5	213	Multiple Kernel Fuzzy C-Means Algorithm with ALS method for Satellite and Medical Image Segmentation Authors: Yugander P, Sheshagiri Babu J, Sunanda K and Susmitha E	1.YUGANDER.P
6	216	Possibilistic Fuzzy C-Means Algorithm for Fingerprint Image Segmentation with ALS Method Authors: Raghotham Reddy G, Yugander P and Sheshagiri Babu J	1.YUGANDER.P
7	265	MORPHOLOGICAL IMAGE PROCESSING APPROACH ON THE DETECTION OF TUMOR AND CANCER CELLS Authors: Ms. M. Parisa Beham, Ms.A.B.Gurulakshmi	1.M. PARISA BEHAM

COMMUNICATION(C2)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	94	A DFT Methodology Targeting On-line Testing Of Reversible Circuit Authors: Bibhash Sen, Jyotirmoy Das and Biplab K Sikdar	1.JYOTIRMOY DAS
2	95	Removal of Radio Irregularity Crisis in WSN localization using Enhanced Co-Ordinate Signal Strength Database Authors: P.Shunmuga Perumal and V.Rhymend Uthariaraj	1.P.SHUNMUGA PERUMAL
3	103	Geographical Location Based Hierarchical Routing Strategy for Wireless Sensor Networks Authors: Pramod Kumar, Ashvini Chaturvedi and M. Kulkarni	1.PRAMOD KUMAR
4	123	Design of Low Power and High Performance Router Using Dynamic Power Reduction Technique Authors: Lakshmi Narayana Thalluri and S R Sastry Kalavakolanu	1.LAKSHMI NARAYANA THALLURI, 2.KRISHNA KARTHIK TATINENI 3.S. R. SASTRY KALAVAKOLANU
5	128	Performance Measures of L-Independent Block Fading Rayleigh Channel with Perfect Channel Estimation for a SISO System Authors : Reshma John and Vidhyacharan Bhaskar	1.RESHMA JOHN
6	131	Evaluation of MUSIC Algorithm for a Smart Antenna System for Mobile Communications Authors: Nageswara Rao Thadikamalla and Srinivasa Rao Vempati	1.T.NAGESWARA RAO 2.V.SRINIVASA RAO
7	148	Analysis of DMT in Multi-User Wireless Network Using Orthogonal, Non-Orthogonal and Cluster MDS FFNC Authors: Sivarajan R, Venkatesan A and Vanitha L	1.SIVARAJAN R
8	156	Near Field Magnetic Induction Communication In Body Area Network Authors: Nithya Thilak and Robin Braun	2.NITHYA THILAK

MEMS/NANO(M2)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	394	An HVD Based Error Detection and Correction of Soft Errors in Semiconductor Memories Used for Space Applications Authors: Shalini Sharma and P. Vijayakumar	1.SHALINI SHARMA
2	397	Partitioning in 3D ICs: A TSV Aware Strategy with Area Balancing Authors: Prasun Ghosal and Soutrik Chatterjee	1.PRASUN GHOSAL
3	195	Analysis of Scattering by Dielectric bodies-Comparison of TLM And FDTD-PML Methods Authors: Srinivasa Rao R, Venkata Subbaiah P and Prabhakar Rao B	1.R.SRINIVASA.RAO
4	206	Evaluation of Branch Predictors Targeting Easeful Diagnosis of Design Inaccuracies Authors: Baisakhi Das, Mousumi Saha and Biplab K Sikdar	1.BAISAKHI DAS
5	221	Efficiency Enhancement of Solar Cell:Fusion of Texturisation and Back Contact Emitter-Wrap-Through modeling Authors: Abu Hanif Md. Ripon, Abu Asraf Siddique, Sk. Md. Golam Mostafa and A B M Rafi Sazzad	1.ABU HANIF MD. RIPON
6	263	A Cellular Automata Based High Speed Test Hardware For Word-Organized Memories. Authors: Mousumi Saha and Biplab K Sikder	1.MOUSUMI SAHA
7	402	Random Dopant Induced Variability in SOI Trigate FINFET : A Simulation Study Authors : Rama Pradeep Reddy G and Bindu Boby	1.RAMA PRADEEP REDDY.G
8	201	SIMULATION STUDY OF SOI FOUR GATE TRANSISTOR Authors : Bishwajit Debnath, M. Sariful Islam, Samantha Lubaba Noor, Muhsiul Hassan, A.F.M. Saniul Haq and M. Ziaur Rahman Khan	1.MUHSIUL HASSAN
8	142	Design of an On Chip Read-out Circuit for Piezo-Resistive MEMS Pressure Sensor M.Santosh, Kanhu Ch Behera, S C Bose	1.M.SANTOSH 2.KANHU. CH. BEHERA 3.S. C BOSE

VLSI(V4)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	154	Effect of Ge-dosing Profile of Exponentially-doped Base on the Internal Quantum Efficiency of a SiGe Solar Cell Authors: Md. Rashedul Huce, H. M. Aziz, K. M. Kolinca, M. S. Uddin and Md. Iqbal Bahar Chowdhury	1.H. M. AZIZ
2	158	LOW POWER ANALYSIS OF TRIPLE GATE MOSFETs Authors: Doreen Joy and Nirmal D	1.DOREEN JOY
3	161	A Novel Average Current-Mode Controller Based Optimal Battery Charger for Automotive Applications Authors: Rajeev Kumar Singh, Nitin Singh Chauhan and Santanu Mishra	1.NITIN SINGH CHAUHAN
4	164	Energy Recovery Clock Gating Scheme And Negative Edge Triggered Flipflop For Low Power Applications Authors: Jennifer Judy D and Kanchana Bhaskaran V S	1.D. JENNIFER JUDY
5	168	A Novel Four Quadrant Cmos Analog Multiplier Authors: Om Prakash Kumar, J. Michel Suman and Mrs. Flavia Princess	1.OM PRAKASH KUMAR
6	170	Design of Micro power CMOS LNA for Healthcare Applications Authors: Manjula Sankar and Selvathi D	1.MANJULA.S
7	184	Thermal Aware Modern VLSI Floor planning Authors: Gracia Rani, Rajarami Siva, Athira Sudarsan and Nivethieha KK	1.NIVETHITHA. K
8	196	An FPGA Implementation of Low Density Parity-Check Codes Construction & Decoding Authors: SUSMITHA REMMANAPUDI & BALAJI BANDARU	1.SUSMITHA REMMANAPUDI
9	208	Enhanced Power Gating Schemes for Low Leakage Low Ground Bounce Noise in Deep Submicron Circuits Authors: Chhavi Saxena, Manisha Pattanaik and R.K Tiwari	1.CHHAVI SAXENA

SESSION 1EMBEDDED SYSTEM(E1)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	70	DESIGN AND CHARACTERIZATION OF MEMS THERMAL ACTUATOR Authors: Veda Sandeep Nagaraja, Pinjare S.L. and Neethu K.N.	1.VEDA SANDEEP NAGARAJA 2.NEETHU K.N
2	192	Zero Delay Clock System in GHz Frequency Regime using CRLH Metamaterial Structure Authors: Soorya Krishna and M S Bhat	1.M.S. BHAT
3	243	Single Phase Clocked Quasi Static Adiabatic Tree Adder Authors: Sasipriya P and Kanchana Bhaaskaran V S	1.SASIPRIYA. P
4	71	Subthreshold Charge Leakage in Nanoparticle Embedded DGMOSFET Memory Devices An Analytical Study Authors: Amretashis Sengupta, Kalyan Koley and Chandan Kumar Sarkar	1.AMRETASHIS SENGUPTA
5	84	A Simple Electronic Analog of the Postsynaptic Authors: Dr. Jiten Ch., Taslima Ahmed	1.TASLIMA AHMED
6	87	Optimal Implementation of UART-SPI Interface of SOC Authors: Praveen Blessington T, Dr Bhanu Murthy B and Venkata Ganesh G	1.T. PRAVEEN BLESSINGTON 2. Dr.BHANU MURTHY
7	135	Gesture Recognition using Field Programmable Gate Arrays. Authors: Alex Raj S.M., Sreelatha G. and Supriya M.H	1.S.M.ALEX RAJ
8	160	Real Time Communication between Multiple FPGA Systems in Multitasking Environment Using RTOS Authors: Rourab Paul, Sangeet Saha, Suman Sau and Amlan Chakrabarti	1.SANGEET SAHA

VLSI(V7)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	318	A Low-Power And High Performance Radix-4 Multiplier Design Authors: Anu Priyadharsini and Jackuline Moni	1.ANU PRIYADHARSINI
2	322	Performance Evaluation of Junctionless Vertical Double Gate MOSFET Authors: Jagdeep Rahul, Anurag Srivastava, Shekhar Yadav and Kamal Kishor	1.JAGDEEP RAHUL
3	325	Design of a 32nm 7T SRAM Cell based on CNTFET for Low Power Operation Authors: Rajendra Prasad Somineni, Dr B K Madhavi and Dr. K Lal Kishore	1.RAJENDRA PRASAD S
4	336	TCAD Assessment of Nonconventional Dual Insulator Double Gate MOSFET Authors: Shekhar Yadav, Anurag Srivastava, Jagdeep Rahul and Kamal Kishore Jha	1.SHEKHAR YADAV
5	341	Design of all-optical New Gate using Mach-Zehnder Interferometer Authors: Goutam Maity, Santi Maity and Jitendra Nath Roy	1.GOUTAM KUMAR MAITY
6	343	All-Optical Manchester Code Generator using TOAD-based D Flip-Flop Authors: Goutam Maity, Santi Maity and Jitendra Nath Roy	1.GOUTAM KUMAR MAITY
7	80	A Technique for Low Power Testing of VLSI Chips Authors: Jayagowri R and Gurusurthy K.S	1.R.JAYAGOWRI 2.K.S.GURUMURTHY
8	348	Performance Analysis Of Three Phase Solid State Transformer Authors: Sujit Tripathy, Rc Mala, Rahul Reddy Devarapally and Savita Tadepalli	1.DEVARAPALLY RAHUL REDDY 2.SUJIT TRIPATHY 3.SAVITA TADEPALLI
9	232	Implementation and Analysis of Power Clock Generation Method for Adiabatic Circuits Authors: Amit Kenjale, Prasad D. Khandekar, Abhijit V. Chitre	1.AMIT KENJALE

VLSI(V5)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	241	Asymmetric Gate Oxide Tunnel Field Effect Transistor for Improved Circuit Performance Authors: Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta	1.RAKHI NARANG
2	242	LATERALLY Asymmetric Channel Insulated Shallow Extension-Silicon-On-Nothing MD-ISE-SON MOSFET For Improved Reliability And Digital Circuit Simulation Authors: Vandana Kumari,Manoj Saxena,R.S .Gupta,Mridula Gupta	1.VANDANA KUMARI
3	246	VLSI Design and Implementation of Reconfigurable OFDM Transcievers for Software Defined Radio Authors: Vamshi Krishna Puram, Prabu S and Logashanmugam E	1. VAMSHI KRISHNA 2.S. PRABU
4	247	Adaptive Transmission for Power Line Communication using Neural Networks Authors: Rathinasabapathy M and Nakkeeran R	1.RATHINASABAPATHY.M
5	248	Impact of Localised Charges Present in the Interfacial Layer of the Schottky Contact in SOI MESFET Authors: Rajni Gautam, Manoj Saxena, R.S. Gupta and Mridula Gupta	1.RAJNI GAUTAM
6	256	Synthesis And Implementation Of 3gpp Lte Physical Downlink Control Channel(Pdcch) Using Fpga Authors: Syed Ameer Abbas, Geethu Karuna Sudhamony and S.J.Thiruvengadam	1.GEETHU K.S
7	268	High Speed and Area Efficient Vedic Multiplier Authors: Vaijyanath Kunchigi, Linganagouda Kulkarni and Subhash Kulkarni	1.VAIJYANATH KUNCHIGI
8	274	Local Clustering and Threshold Sensitive routing algorithm for Wireless Sensor Networks Authors: Roseline R A and Sumathi P	1.R.A.ROSELINE
9	220	High-Speed and Low-Power Dynamic Latch Comparator Authors: Jisha P and Dr.Jackuline Moni	1.JISHA P

COMMUNICATION(C3)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	167	IMPROVED PERFORMANCE OF UDP & TCP THROUGHPUT IN Wi-Fi NETWORKS FOR VOICE AND DATA SERVICES IN MOBILE COMMUNICATIONS WITH MIMO SYSTEMS Authors: Venkat Ramana P and Dr. Narayana Reddy S.	1.P.VENKAT RAMANA
2	171	Fuzzy Extended Kalman Filter to Estimate Rayleigh Fading Channel with PSAM for MIMO-OFDM Authors: Rajendra Prasad Kondaveeti and Naga Harshavardhan Kolisetty	1.RAJENDRA PRASAD K
3	175	Correlation Properties and Performance Evaluation of 1-Dimensional OOC's for OCDMA Authors: Joseph Ofosuhene Anaman and Shanthi Prince	1.ANAMAN JOSEPH OFOSUHENE
4	191	A Study on Inter-satellite Optical Wireless Communication and its Performance Analysis Authors: Michael Rani and Shanthi Prince	1.MICHAEL RANI
5	244	Comparison of Platform Independent Electronic Document Distribution Techniques Authors: Diwakar R. Marur and Vidhyacharan Bhaskar	1.DIWAKAR R. MARUR
6	266	The optimum signal perturbation free transmit scheme to enhance the channel estimation of MIMO-OFDM system Authors: R.Jeyanthi and Dr.N.Malmurugan	1.R.JEYANTHI
7	321	High-Speed and Low-Power ASIC Implementation of OFDM Transceiver based on WLAN (IEEE 802.11a) Authors: Mamidi Nagaraju and Rakesh Madala	1.MAMIDI. NAGARAJU

VLSI(V6)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	277	VLSI Design Of Power Efficient Carry Skip Adder Using Tsg & Fredkin Reversible Gate Authors: Sujata Chiwande and Pravin Dakhole	1.SUJATA S. CHIWANDE
2	288	Design and Implementation of Demodulation Technique with Complex DPLL using CORDIC Algorithm Authors: Vinoth S, Sathish Kumar M and Vanitha L	1.VINOTH. S.
3	291	Effect of Parameter Optimization Effort over MOSFET Models' Performances in Analog Circuits' Simulation Authors: Deepak Balodi, Chumki Saha and P. A. Govidacharyulu	1.DEEPAK BALODI
4	294	Analysis and Modeling of 1/f Noise in MOSFETs: The Joint Effect of Channel Length and Channel Resistance Authors: Hardev Singh, Rakesh Sarin and Sarbjeet Singh	1.HARDEV SINGH
5	302	Highly Secured High Throughput VLSI Architecture for AES Algorithm Authors: M Vanitha and R Sakthivel	1.M.VANITHA
6	315	Low-power dissipation using FPGA Architecture Authors: Balaji Muthusamy, Vijayan Subrahmaniam	1.SUNDAR PRAKASH BALAJI MUTHUSAMY
7	316	FPGA Implementation of Neural Network for Linearization of Thermistor Characteristics Authors: Durlav Sonowal and Manabendra Bhuyan	1.DURLAV SONOWAL
8	227	MULTI-SRAM Reducing Power Through Recovery-Boosting Authors: Himani Kaushal, Eswaran P	1.HIMANI KAUSHAL

SESSION 2

IMAGE PROCESSING(I3)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	217	Image Compression Using Multidirectional Anisotropic Transform: Shearlet Transform Authors: S Thayammal and D Selvathi	1.S.THAYAMMAL
2	239	Fingerprint Generation of Audio Signal Using Difference of Gaussian Authors: M. Davidson Kamaladhas and Abitha V	1.V. ABITHA
3	252	Statistical Modeling for the Characterization of Atheromatous Plaque in Intravascular Ultrasound Images Authors: Selvathi D and Emimal N	1.EMIMAL N
4	253	Detection of Retinal Blood Vessels Using Curvelet Transform Authors: Selvathi D and Neethi Balagopal	1.NEETHI BALAGOPAL
5	254	A SECURE CRYPTOSYSTEM FOR IMAGE ENCRYPTION Authors: Rithmi Mitter and M Sridevi Sathya Priya	1.RITHMI MITTER
6	259	Object Recognition based on Gabor Wavelet Features Authors: Ahila Priyadarshini, Dr Arivazhagan.S & Seedhanadevi S	1.S.SEEDHANADEV I
7	329	PERFORMANCE EVALUATION OF IMAGE COMPRESSION TECHNIQUES Authors: Abhishek Bhardwaj and Asheesh Kumar	1.ABHISHEK BHARDWAJ

COMMUNICATION(C4)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	337	Extended Kalman Filter based Estimation for Fast Fading MIMO Channels Authors: George Ignatius, Murali Kirshna Varma U, Nitish S Krishna and Sachin Pv	1.GEORGE IGNATIUS
2	361	Spectrum Efficiency of Nakagami-m Fading Channels for SISO System in the Presence of Adjacent Channel Interference for various Adaptation Policies Authors: Gokulakrishnan Radhakrishnan and Vidhyacharan Bhaskar	1.R. GOKULAKRISHNAN
3	365	Efficient Spectrum Sensing Methods For Cognitive Radio Networks Authors: Rajeswari A and Dhaarani T G	1.T.G.DHAARANI
4	375	Dual Polarized Circular Microstrip Space-fed Antenna Array Design with High Isolation and Broad Bandwidth Authors: Prashant Kumar Mishra and Girish Kumar	1.PRASHANT KUMAR MISHRA
5	395	Integration of Vehicular Roadside Access and the Internet: Challenges & a Review of Strategies Authors: Mohd Umarfarooq	1.MOHD UMAR FAROOQ
6	405	Design approach of throughput improvement for cellular network Authors: Satish Kumar V M.Tech, Sridhar Reddy K, Maheswarareddy, Ashok Kumar	1.SATISH KUMAR V
7	406	Novel Number Allotment method with UTNA (Unique Token Number Allocation) Security System for Mobile User Authors: Puneet Sachdev, Mr. Ashutosh Kumar Dubey	1.ASHUTOSH KUMAR DUBEY
8	407	A Novel Approach Based on PN Sequence coding for Reduction of Peak to Average Power Ratio (PAPR) in Orthogonal Frequency Division Multiplexing (OFDM) Authors: Ms. Manisha Rathore, Ms. Pooja Rajotiya, Mr. Saket Kumar, Mr. Animesh K. Dubey, Mr. Ashutosh Kumar Dubey	1.ASHUTOSH KUMAR DUBEY

SIGNAL PROCESSING(S1)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	60	Multi-View Distributed Video Coding Authors : Kodavalla Vijay Kumar and P G Krishna Mohan	1.VIJAY KUMAR KODAVALLA
2	90	Signal processing and channel capacity enhancement using MIMO Technology Authors: Akhilesh Kumar, Abhay Mukherjee, Kamata Nath Mistra and Anil Chaudhary	1. ANIL KUMAR CHAUDHARY
3	180	An Efficient and Simple Audio Watermarking Using DCT-SVD Authors : Suresh Gulivindala, N V Lalitha, Chanamallu Srinivasa Rao and V Sailaja	1.GULIVINDALA SURESH
4	181	Robust Speaker Identification using Vocal Source Information Authors : R Shantha Selva Kumari, S Selva Nidhyananthan and G Jaffino	1.G.JAFFINO
5	189	Speech Enhancement Using Kalman Filter for white, random and color noise Authors : Mariyadasu Mathe, Sivaprasad Nandyala and Dr.T.Kishore Kumar	1.T. KISHORE KUMAR
6	299	Determination of the Peak Power Voltage Using Explicit PLM of an Illuminated Solar Cell; Authors: Abhik Kumar Das	1.ABHIK KUMAR DAS
7	313	Chroma Components Coding Method in Distributed Video Coding Authors : Vijay Kumar Kodavalla and P.G Krishna Mohan	1.VIJAY KUMAR KODAVALLA

IMAGE PROCESSING(I4)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	330	Feature Preserving Super-resolution : Use of LBP and DWT Authors: Parul Pithadia, Prakash Gajjar and Janardan Dave	1.PARUL V. PITHADIA
2	340	Analysis of B-Mode Transverse Ultrasound Common Carotid Artery Images using Contour Tracking by Particle Filtering Technique Authors: Thangavel M, Chandrasekaran M and Madheswaran M	1.M.THANGAVEL
3	372	Score Level Fusion of SIFT and SURF for Iris Authors: Sambit Bakshi, Sujata Das, Hunny Mehrotra and Pankaj K Sa	1.SAMBIT BAKSHI
4	374	Man-made Object Classification in SAR Images Using Gabor Authors: Vasuki Perumal and Dr.S.Md.Mansoor Roomi	1.P. VASUKI
5	396	Massive Stream Data Processing to Attain Anomaly Intrusion Prevention Authors: Kavitha C and Suresh M	1.M. SURESH 2.C. KAVITHA
6	403	SMS Compression Using Arithmetic Coding Modification Authors: Pravin Kumbhar and Shoba Krishnan	1.PRAVIN Y KUMBHAR 2.SHOBA KRISHNAN

VLSI(V8)

S.NO	PAPER ID	TITLE	REGISTERED AUTHORS
1	351	Computing Greatest Common Divisor of two positive integers using SET-MOS Hybrid Architecture Authors: Debasis Samanta, Subir Kumar Sarkar and Asish Kumar De	1.DEBASIS SAMANTA
2	354	An Efficient Test Design for CMPs Cache Coherence Authors: Mamata Dalui and Biplab K Sikdar	1.MAMATA DALUI
3	356	A Cellular Automata Based Test Scheme for TSVs in 3D ICs Authors: Bidesh Chakraborty and Mamata Dalui	1.MAMATA DALUI
4	359	Variable Gate Oxide Thickness MOSFET: A Device level solution for Sub-threshold Leakage current reduction Authors: Keerti Kumar Korlapati and Bheema Rao N	1.K. KEERTI KUMAR
5	360	Fully Parallel and Fully serial architecture for realization of high speed FIR Filters with FPGA's Authors: V.SUDHAKAR, N.S.MURTHY, L.ANJANEYULU	1.V.SUDHAKAR
6	364	A Two Dimensional Analytical Modeling of Fully Depleted Dual Material Gate SON MOSFET and Evidence for Suppressed SCEs Authors: Sounak Naha, Saheli Sarkhel and Subir Kumar Sarkar	1.SUBIR KUMAR SARKAR
7	369	TOAD-based All-Optical Gold Code Generator Authors: Goutam Maity, Santi Maity and Jitendra Nath Roy	1.GOUTAM KUMAR MAITY
8	376	FPGA Design of a Fast 32-bit Floating Point Multiplier Unit Authors: Ajit Kumar Panda, Muchharla Suresh, Anna Jain and Baisakhy Dash	1.ANNA JAIN 2.BAISAKHY DASH

Instructions for Presentation

- 1. Total time for a participant: 11 minutes**
Presentation time: 8 minutes + Question time: 3 minutes
- 2. Number of slides: 10 to 12 slides**

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